26.5 2Mb Spin-Transfer Torque RAM (SPRAM) with Bit-by-Bit Bidirectional Current Write and Parallelizing-Direction Current Read

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Spin-transfer torque writing type memory is a viable candidate for low power non-volatile RAM or universal memory [5]. It features a magnetic tunnel junction with MgO tunneling barrier [1,2], with a tunnel magnetoresistance (TMR) ratio (i.e., ratio of '1' state to '0' state) of over 100% (up to 472% [3]) and reduced threshold current (write current) density under 500μA per cell (down to 100μA [4]). So far, however, there are few reports of circuits and memory-array technology that are appropriate for spin-transfer torque writing and its related reading schemes. Here, we describe the circuit and array technologies for a 1.8V 2Mb spin-transfer torque RAM (SPRAM) fully functional chip (except for test mode and redundancy). This chip features an array scheme with bit-by-bit bidirectional current write, achieving proper spin-transfer torque writing of 100ns, and a parallelizing-direction current read with 0.7V bitline voltage to make it immune to read disturbance. The SPRAM has a 40ns access time in a 0.2μm process.

The array configuration of the 256kb sub-array is shown in Fig. 26.5.1. The 256kb array consists of two 128kb arrays in which bitlines (BL) and source-lines (SL) are feed into 16:1 muxes, controlled by BS, to share the write driver and sense amp/latch circuits. Each selector, shown as a switch in this figure, is actually composed of analog switch and discharge circuits for grounding of unselected lines. The sense amp/latch is activated by SAE and its output of SALT and SALB are connected to the I/O line by a YS signal and also enters to the write driver. This circuit is used as a latch circuit in writing and as a sense amplifier in reading. By conforming connection to BL and SL by WER or WEL, the write driver controlled by WEM can handle one side of the two 128kb arrays in writing. In reading, an open-bit architecture is adopted by RE which uses both 128kb arrays with dummy cells. The reading data is inverted according to which side of the 128kb array it is associated. Dummy cells with word lines of DWL or DWR and VM to control the current are located by one line in each 128kb array.

The most important feature of spin-transfer torque writing is the direction of current through a memory cell, which determine the data written to the cell. The cell writing current and writing time are symmetrical between '1' and '0'. Thus, the write driver needs to have symmetrical bidirectional current flow capabilities, so it must be both a current source and current sink. As seen in the circuit diagram of Fig. 26.5.2, this function is implemented as a current direction selector with WE-controlled flip-flop circuits, the state of which is determined by the output of the latch circuit, SALT/SALB. These outputs are connected to switched inverter type circuits.

The operation of bidirectional symmetrical current read is composed of '0' or '1' data load and corresponding write as shown in the timing diagram of Fig. 26.5.3(a). First, the data for latch circuits are transferred from the I/O line (also shown in Fig. 26.5.3(b)). When SALT is 'H' and SALB is 'L', '0' write (parallelizing) operation is started (Fig. 26.5.3(c)). Wordline W_i is selected and BL is connected to the write driver by BS0 and WER, and WEM activates the write driver. The PMOS in the driver connected to the bitline is in the ON state and acts as a current source, and the NMOS in the driver connected to the source-line is in the ON state and acts as a current sink. In this way, the current flows from the upper (free layer) to the lower (pinned layer), injecting the majority of spin electrons of the pinned layer to the free layer. This results in spin-transfer torque, making the free-layer magnetizations parallel to the pinned layer, i.e., the flowing current parallelizes the spin in the free layer to the pinned layer. The '1' write (anti-parallelizing) after data loading is seen in Fig. 26.5.3 (d). Here, since the levels of SALT and SALB are inverted, the driver connected to the bitline is the current sink, and the driver connected to the source-line is the current source. The reflected electrons spin in an anti-paralleled direction, exerting torque onto the free layer's magnetization and making it anti-parallel to that of the pinned layer.

An open-bit scheme is used for reading: the latch circuits in the write operation are used as a sense amplifier, as shown in Fig. 26.5.4(a). Here the source-lines of the two arrays are connected to ground and there is a dummy cell in the left and right arrays. By controlling the voltage of VM, the dummy-cell resistance is adjusted to reach the middle of the parallel and anti-parallel states for a wide temperature range. The reading data is amplified and emerged at SALT and SALB. Here, there are two current directions for a memory cell in reading: parallelizing direction and anti-parallelizing directions (as shown in Fig.26.5.4(b)). The memory cell has two states of resistance values corresponding to the direction of magnetization in the free layer with respect to that of the pinned layer. When they are parallel, the cell is in the low resistance state, R_P, and when they are anti-parallel, the cell is in the high resistance state, R_{AP}. The R_{AP} resistance depends on the reading current, as shown in Fig. 26.5.4(c). The magnitude of R_{AP} decreases with reading current. In this chip, parallelizing direction reading is chosen because this reading is immune to unwanted reversal of magnetization. The disturbance occurs when we read the R_{AP} state in this reading, where the current is low and moves to the lower side with increasing the TMR ratio.

The distance between the reading point and the trip point of parallel sate, Disturb AP in Fig. 26.5.4(c), shows the amount of immunity to disturbance. This is larger than the opposite case. In anti-parallelizing reading, although the threshold current is rather large, large reading current is close to the trip point of the anti-parallel state (Disturb P). Therefore, we use parallelizing direction reading. Also to further prevent disturbance, bitline voltage in reading is as low as possible. However, low-voltage generally means degraded signals. The dependence of the TMR ratio on the reading current, on the other hand, indicates that less current causes a larger TMR ratio, i.e., a large signal as shown in Fig. 26.5.4(d). High-speed operation with a low bitline voltage is possible by using this feature. With measured TMR dependence, Fig. 26.5.5(a) indicates that a bitline voltage of 0.6 to 0.7V is preferable for large signal current. The simulated results for reading using this low bitline voltage reveal that the clock input to SA output is 32ns (Fig. 26.5.5(b)), a read access time of 40 ns is expected, including the I/O buffer.

A transmission electron micrograph (TEM) of the TMR pillar used in the memory cell is shown in Fig. 26.5.6(a). The MgO thickness is 1.0nm and the free layer is made of CoFe(1.0nm)/NiFe(2.0nm). Fig. 26.5.6(b) shows early measurements of R-I curves with repeated 100ns writing. There is no degradation after 10^9 cycles. A chip micrograph and chip features are shown in Fig. 26.5.7. The chip is fabricated in a 0.2μm logic process and the memory cell uses upper metal with 0.4μm line and 0.4μm space rules.

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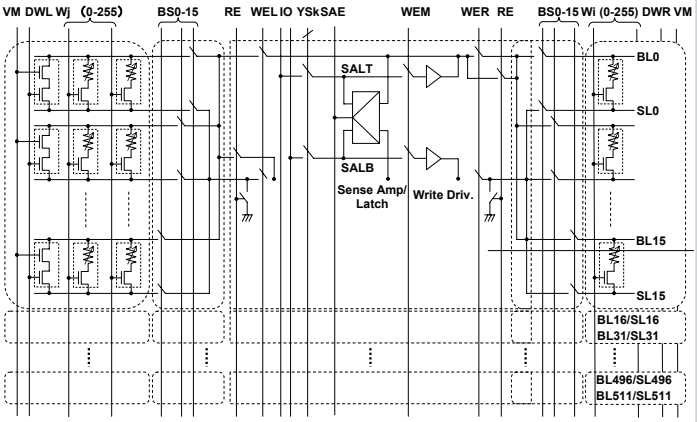

Figure 26.5.1: 256kb sub-array scheme.

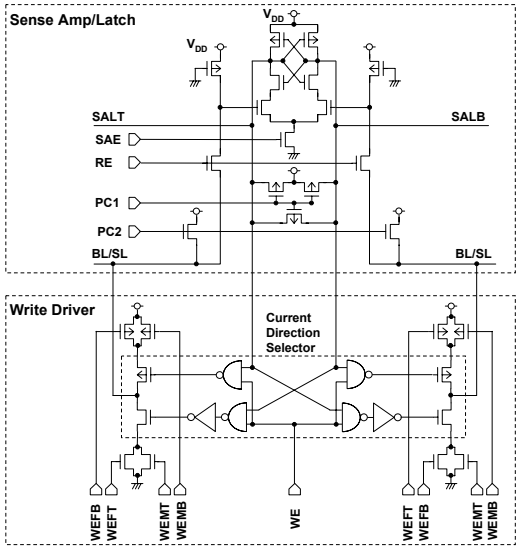

Figure 26.5.2: Sense amp/latch and write driver.

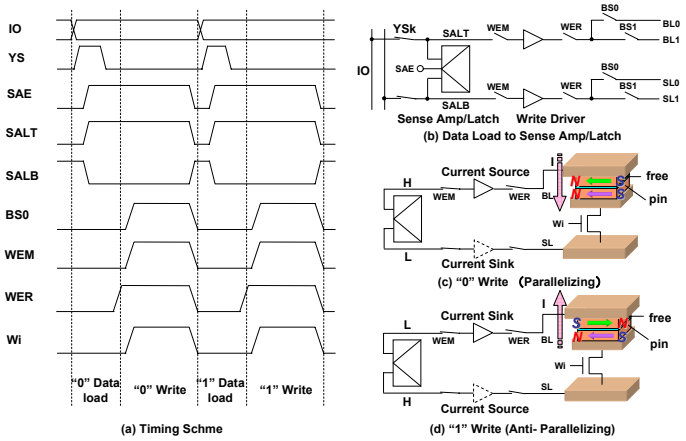

Figure 26.5.3: Bi-directional symmetrical current write.

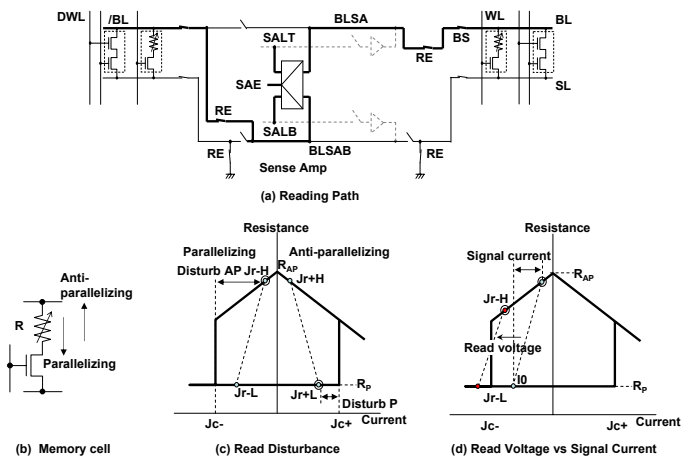

Figure 26.5.4: Parallelizing-direction current read.

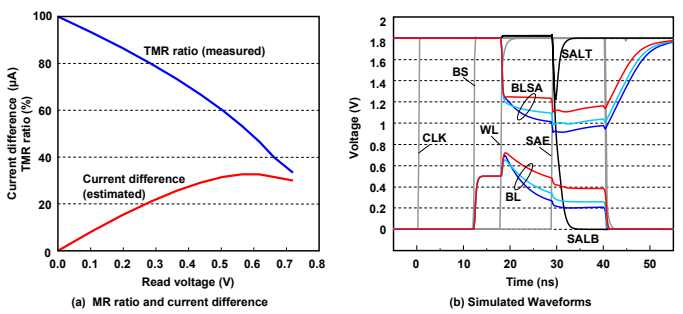

Figure 26.5.5: High-speed read with low-voltage bitline.

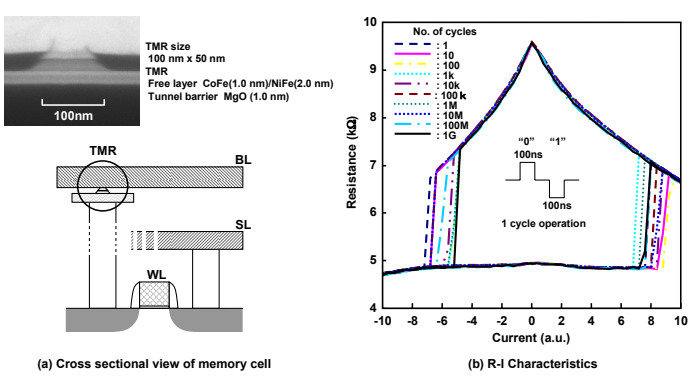

Figure 26.5.6: Cell structure and R-I characteristic.

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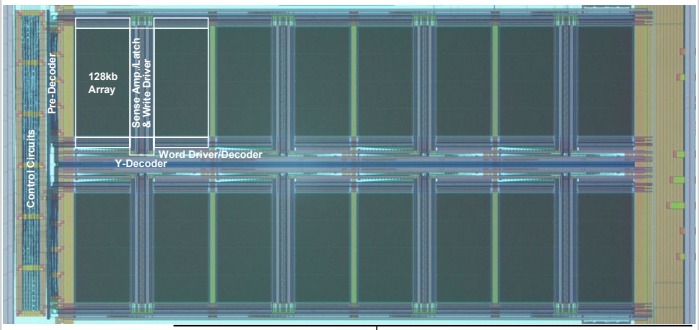

Features

Density		2Mb
Process		0.2μm CMOS, 1 Poly, 4 Metal
Memory Cell size		1.6x1.6μm² (designed under 0.4μm upper metal L/S)
Power Supply		1.8V
Write	Cell Current	200μA
	time	100ns
Read	time	40ns
Chip Module size		5.32x2.50mm²

Figure 26.5.7: Chip micrograph and features.

